CLAIMS

WHAT IS CLAIMED:

1. A semiconductor structure, comprising:

a dielectric layer;

a metal region formed in said dielectric layer having a first surface portion and a second surface portion opposite to said first surface portion; and

a dielectric cap layer formed on said first surface portion of said metal region, said dielectric cap layer and said first surface portion forming an interface;

wherein a concentration of diffusion rate reducing material within said metal region at said first surface portion is higher than at said second surface portion.

2. The semiconductor structure of claim 1, wherein said metal region is comprised of copper.

3. The semiconductor structure of claim 1, wherein said cap layer comprises at least one of silicon, carbon and nitrogen.

4. The semiconductor structure of claim 1, wherein a thickness of said cap layer is in the range of approximately 10-70 nm.

5. The semiconductor structure of claim 1, wherein said diffusion rate reducing material in said metal region is a dielectric material.

6. The semiconductor structure of claim 5, wherein said dielectric material comprises material that is contained in said cap layer.

7. The semiconductor structure of claim 1, wherein a maximum concentration within said metal region of said diffusion rate reducing material is located within a distance of approximately 20 nm from said interface.

8. The semiconductor structure of claim 7, wherein said maximum concentration of said diffusion rate reducing material is located within a distance of approximately 10 nm from said interface.

9. The semiconductor structure of claim 7, wherein said concentration of said diffusion rate reducing material in said metal region decreases with an increasing distance from said interface.

10. The semiconductor structure of claim 1, further comprising a conductive barrier layer that is in contact with sidewalls and said second surface portion of said metal region.

11. The semiconductor structure of claim 1, wherein said metal region is a portion of a metallization layer connecting a plurality of circuit elements.

12. The semiconductor structure of claim 11, wherein said metal region is a metal line having a lateral dimension of less than 130 nm.

13. A method, comprising:

forming a metal region above a substrate, said metal region comprising a first surface portion and a second surface portion opposite to said first surface portion;

forming a cap layer on said first surface portion; and

implanting a diffusion rate reducing material into said metal region.

14. The method of claim 13, further comprising adjusting implantation parameters on the basis of a material composition of said metal region and said cap layer and on the basis of a thickness of said cap layer so as to locate a peak concentration within said metal region of said diffusion rate reducing material within approximately 20 nm of an interface formed by said first surface portion and said cap layer.

15. The method of claim 14, wherein said implantation parameters are selected so as to locate said peak concentration within a distance of approximately 10 nm from said interface.

16. The method of claim 13, wherein said metal region comprises copper.

17. The method of claim 13, further comprising forming a second cap layer on said cap layer after the implantation of said diffusion rate reducing material.

18. The method of claim 13, further comprising removing at least a portion of said cap layer after the implantation of said diffusion rate reducing material.

19. The method of claim 18, further comprising forming a second cap layer after removal of at least a portion of said cap layer.

20. The method of claim 13, wherein said diffusion rate reducing material is a dielectric material.

21. The method of claim 20, wherein said dielectric material comprises a material contained in said cap layer.